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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/234,427	01/20/1999	AMOS INTRATER	NSC8-8400	6107

33402 7590 09/29/2005

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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/234,427	INTRATER ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,18,27 and 36-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-8* is/are allowed.

6)☒ Claim(s) *18,27 and 36-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 18,27,36-39 are presented for examination. Claims 1,9,10 have been canceled. S.N. 08/317,783 is the application number for the surrendered patent 5,630,153. Claims 11-17, 19-26,28-35 and 40-44 have been canceled. Claims 11,20,and 29 have been canceled in paper # 2. Claims 2-8 are allowable over the art of record.

2. Upon further review and consideration with special examination, The following is applicable to currently presented claims 18,27,36-39. This is a non-final action to allow applicant to respond. This action supersedes all previous actions.

3. Claims 18,27, 36 (claims 18,27,36 included limitations of canceled claims 11,20,29) are rejected under 35 U.S.C. 251 as being an improper recapture of broadened claimed subject matter surrendered in the application for the patent upon which the present reissue is based. See *Hester Industries, Inc.* v. *Stein, Inc.*, 142 F.3d 1472, 46 USPQ2d 1641 (Fed. Cir. 1998); *In re Clement,* 131 F.3d 1464, 45 USPQ2d 1161 (Fed. Cir. 1997); *Ball Corp.* v. *United States*, 729 F.2d 1429, 1436, 221 USPQ 289, 295 (Fed. Cir. 1984). A broadening aspect is present in the reissue which was not present in the application for patent. The record of the application for the patent shows that the broadening aspect (in the reissue) relates to subject matter that applicant previously surrendered during the prosecution of the application. Accordingly, the narrow scope of the claims in the patent was not an error within the meaning of 35

U.S.C. 251, and the broader scope surrendered in the application for the patent cannot be recaptured by the filing of the present reissue application.

4. As to reissue claims 18, 27, claim 18 was dependent from canceled claim 11, and now presented in independent form. Likewise, claim 27 was dependent from canceled claim 20, and now presented in independent form . Claims 18 , 27 additionally recite the feature of DSP only execute a single instruction when the information is loaded into the register. However, this feature of execution of single instruction when the information is loaded into the register is directed to the extract element which is not related to the surrender subject as set forth in 1412.02 (a), reissue claim is narrower than patented claim in area not directed to the amendment or argument to over come the rejection. For example, regarding claim 18 (claims 18, 27 included limitations of canceled claims11, 20 , respectively) , applicant indicated in Paper #34 that claim 28 (claim 27 by applicant and corrected by Examiner as claim 28 in Paper 34, now claim 7 in the patent) included the combined features of canceled claim 5 which had previously been rejected under A103" as unpatentable over Davis et al. (4,991,169) in view of Doornink et al. (5,185,599) , and claim 6 objected ,respectively, as set forth in Paragraphs V and X in Paper # 31. The limitations of canceled claims 5,6 which were recited in claim 28 in Paper # 34 was used to obviate the rejection. The feature of the first bus (reissue claim 18 , line 3, see also canceled 11 , claim 18 included limitations of claim 11) is the broadening feature of a shared internal bus (Patent claim 7, paragraph c), and Aa memory connected to the first bus≅ (reissue claim 18, see also canceled claim 11, line 3 for reference purpose) is the broadening

feature of a shared internal memory array connected to the shared internal bus≅ (patent claim 7, paragraph d).

5. The omitted features are :

a) the selection of the sequence of DSP instructions for execution by the digital signal execution unit from set of DSP instructions and that perform general purpose processing tasks by executing the general purpose instructions (see claim 7, line 14);

b)transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected (claim 7, lines 16-18);

c)shared memory array accessible by the digital signal execution unit via the internal input and output port for transferring operand utilizable by digital signal execution unit between the shared internal memory array and the digital execution unit the shared internal bus and such that the shared internal memory is accessible by general purpose processor via the internal input and output port for transferring the general purpose instructions and the selected data between the shared internal memory and the general purpose processor on the internal bus (See claim 7, lines 21-33);

c)the shared interface unit recited in claim 7, lines 34-44).

6. Although the reissue claim 18 (see also canceled claim 11 for reference purpose) presented additional feature of starting execution of an instruction in response to the general purpose processor loading information into a register (see reissue claim 18, line 8-10, see also identification of the instruction in claim 27, last line, see also canceled claim 20 for reference purpose, claim 27 included limitations of claim 20), these features are not related to the prior art rejection and not related to the subject

matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

7. Similarly, the newly added feature of execution of single instruction when the information is loaded into the register as set forth in newly presented claims 18, 27 is not related to the prior art rejection and not related to the subject matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

8. As to claim 36 (claim 36 included limitations of claim 29), (As to claim 29), applicant indicated in Paper #34 that claim 29 (claim 28 by applicant and corrected by Examiner as claim 29 in Paper 34, now claim 9 in the patent) included a the combined features of canceled claim 5 which had previously been rejected under A103" as unpatentable over Davis et al. (4,991,169) in view of Doornink et al. (5,185,599) , and claim 20 objected ,respectively, as set forth in Paragraphs V and X in Paper # 31. The limitations of canceled claims 5,20 which were recited in the newly presented claim 29 in Paper # 34 was used to obviate the rejection. The feature of the first bus (reissue claim 29 , line 2) is the broadening feature of Ashared internal bus≅ (Patent claim 9, paragraph c), and Aa memory connected to the first bus≅ (reissue claim 29, line 3) is the broadening feature of Aa shared internal memory array connected to the shared internal bus (patent claim 29, paragraph d).

9. The omitted features are :

a) the selection of the sequence of DSP instructions for execution by the digital signal execution unit from set of DSP instructions and that perform general purpose processing tasks by executing the general purpose instructions (see patent claim 9, paragraph b);

b)transferring both data and instructions and to which both the digital signal execution unit and the general purpose processor are connected (claim 9, paragraph c);

c)shared memory array accessible by the digital signal execution unit via the internal input and output port for transferring operand utilizable by digital signal execution unit between the shared internal memory array and the digital execution unit the shared internal bus and such that the shared internal memory is accessible by general purpose processor via the internal input and output port for transferring the general purpose instructions and the selected data between the shared internal memory and the general purpose processor on the internal bus (See claim 9, paragraph d);

c)the shared interface unit recited in claim 9, lines 20-23);

d)the retrieval of the operands from the shared memory array via shared internal bus for use by the digital execution unit in executing the selected sequence of DSP instructions (patent claim 9, lines 20-24).

10. Although the reissue claim 36 (see also canceled claim 29 for reference purpose) presented additional feature of Aexecuting an instruction in response to GPP loading information into the register (see claim 36, line 8-9), this feature is not related to the prior art rejection and not related to the subject matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

11. Similarly, the newly added feature of execution of single instruction when the information is loaded into the register as set forth in newly presented claim 36 is not related to the prior art rejection and not related to the subject matter surrendered in the original application. Therefore, impermissible recapture of the subject matter exist.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 18, 28,36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parruck et al. (4,799,144) In view of Akagi et al. (4,467,414) in view of Boddie et al. (4,539,635) .

13. Parruck disclosed a data processing system (e.g. see overview in fig.1, and the DSP in fig.6) comprising at least :

a)a first bus (fig.1 [26]);

b)a memory [18] connected to the first bus ;

c)a general purpose processor [on board processor] connecting to the first bus (see fig.1[14]);

d)a digital signal processor [16] connected to the first bus, the dsp having a memory [RAM] and starting execution of instructions in response to the general purpose processor [14] loading information into the memory [RAM] (e.g. see col.6, lines 49-60).

14. As to claims 18, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] as recited in applicant claim 11, line 5. Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col2, lines 15-22). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at memory access level , and Parruck did show the need for loading the operands into the memory by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

15. Neither Parruck nor Akagi specficaaly teaches the execution of single instrcuion as claimed. However, Boddie disclosed that operation could be realized in a signal digital processing with the use of one or more instructions (see col.18, lines 7-15). It would have been obvious to one of ordinary skill in the art to use Boddie in Parruck for executing a single instruction as claimed because the use of Boddie could provide Parruck the ability of processing the digital signal operations in a predefined format, such as a single instruction, thereby reducing the reading cycle of additional instructions, and therefore, reducing the overall latency of the system, and it could be readily done by configuring the single instruction of Boddie into Parruck with modified control parameters (e.g. the instruction length or type) so the single instruction of Boddie could be recognized by Parruck in order to achieve the enhanced overall efficiency, and for doing so, provided a motivation.

16. As to claim 27, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] as recited in applicant claim 20, line 5. Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col2, lines 15-22). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at memory access level , and Parruck did show the need for loading the operands into the memory by disclosing the loading of the necessary

information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

17. Neither Parruck nor Akagi specficaaly teaches the execution of single instrcuion as claimed. However, Boddie disclosed that operation could be realized in a signal digital processing with the use of one or more instructions (see col.18, lines 7-15). It would have been obvious to one of ordinary skill in the art to use Boddie in Parruck for executing a single instruction as claimed because the use of Boddie could provide Parruck the ability of processing the digital signal operations in a predefined format, such as a single instruction, thereby reducing the reading cycle of additional instructions, and therefore, reducing the overall latency of the system, and it could be readily done by configuring the single instruction of Boddie into Parruck with modified control parameters (e.g. the instruction length or type) so the single instruction of Boddie could be recognized by Parruck in order to achieve the enhanced overall efficiency of the reduced instruction cycle, and for doing so, provided a motivation.

18. Parruck did not explicitly show the identification of the instruction as claimed. However, Parruck taught that any new application program could be easily implemented into his system by only introducing a new software (e.g. see col.5, lines 29-33). Therefore, Parruck must have a control to distinguish and identify the new program (the instructions) from the already existed program instructions. Otherwise, the introduction of new software would not be possible. And , for this reason it would have been obvious to one of ordinary skill in the art to identify instructions in a memory system , such as the Parruck's, as claimed (see the reason just set forth above).

19. As to claims 36,, Parruck did not clearly show that his general purpose processor [14] was loading operands into the memory [18] (claim 29, line 5) and retrieving the operands (claim 29, line 10). Instead, Parruck taught the loading of necessary information into the memory [18] for running particular application program (e.g. see col.6, lines 42-45). However, Akagi disclosed a system for loading operands into a memory necessary for operation (e.g. see col.2, lines 15-22), and retrieving the operand (see the reading out request of the operand in col.5, lines 30-37, col.8, lines 57-60, col.10, lines 15-21). It would have been obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into a memory, and retrieving the operand as claimed because the use of Akagi could enhance the memory control of Parruck to store particular type of operands at desired access level , and Parruck did show the need for loading the operands into the memory and retrieving the operands by disclosing the loading of the necessary information into the memory to run a particular application program (e.g. see col.6, lines 50-53), as already known, opcodes and

operands were building elements of programming instructions which were necessary information for running application, and Akagi could be easily implemented into Parruck by modifying the format of instruction operands of Akagi such that it would be recognizable by the access control of the general purpose processor of Parruck, such as read/write operations. Therefore, for the reasons discussed above, it would have bee obvious to one of ordinary skill in the art to use Akagi in Parruck for loading operands into the memory as claimed.

20. Neither Parruck nor Akagi specficaaly teaches the execution of single instrcuion as claimed. However, Boddie disclosed that operation could be realized in a signal digital processing with the use of one or more instructions (see col.18, lines 7-15). It would have been obvious to one of ordinary skill in the art to use Boddie in Parruck for executing a single instruction as claimed because the use of Boddie could provide Parruck the ability of processing the digital signal operations in a predefined format, such as a single instruction, thereby reducing the reading cycle of additional instructions, and therefore, reducing the overall latency of the system, and it could be readily done by configuring the single instruction of Boddie into Parruck with modified control parameters (e.g. the instruction length or type) so the single instruction of Boddie could be recognized by Parruck in order to achieve the enhanced overall efficiency, and for doing so, provided a motivation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parruck et al. (4,799,144) in view of Davis et al. (4,991,169).

22. As to claims 37-39, Parruck taught at least :

a) digital signal processing unit (DSP) that included digital data by executing an algorithm that included a sequence of DSP operations (see DSP 16);

b) general purpose processor [GPP] that selected the sequence of DSP operations for execution by the DSP from a set of DSP operations (see the selected option program in col.5, lines 50-60, col.6, lines 41-60), and performed general purpose operations using selected instruction and data (see fig.1 [14] , see the onboard processor 14);

c) a bus (fig.1 [26])connected to both DSP and general purpose processor ;

c) a memory [RAM] connected to the bus accessible by the DSP for loading instructions and data required by the general purpose processor and the DSP (see the loading of the instructions loaded from motherboard to the on0bord processor col.6, lines 22-36, see also col.6, lines 37-41, for DSP , see also col.6, lines 41-60).

d) Parruck did not specifically show the control register for invoking a DP operation by issuing a command directly to the control register as claimed. However, Davis . However, Davis disclosed command register [213] for monitoring DSP processors

by a host (see col. 13, lines 19-22). It would have been obvious to one of ordinary skill in the art to use Davis in Parruck for including the control register for issuing the command to the control register as claimed because the use of Davis could provide the capability of the general purpose processor of Parruck to accept specific operation command of the DSP at a register level , and therefore increasing the control ability of the general purpose processor over the DSP processor, and it could be readily achieved by predefining the command register (i.e. the control register) of Davis into Parruck with modified control parameters (e.g. the command selection and register type) etc) so that the control register of Davis could be recognized by Parruck in order to provide the enhanced register command capability, and in doing so, provided a motivation.

23. Claim 2 is allowable over the art of record for reciting among all limitations the transfer of the general purpose instructions to digital signal execution unit from the shared external memory via the shared the internal bus.

24. Claim 7 is allowable over the art of record for reciting among all limitations the shared bus interface connected between the shared internal bus and the shared external bus that stores data, instructions and operands.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

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